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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,671	01/16/2004	Chyiu Hyia Poon	CS03-015	8619

7590 08/09/2005

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EXAMINER	
LINDSAY JR, WALTER LEE	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/759,671	POON ET AL.
	Examiner	Art Unit
	Walter L. Lindsay, Jr.	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Amendment filed on 5/31/2005.

Currently, claims 1-26 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

2. The amendment filed 5/31/2005 in App No. 10/759,671 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "Laser parameters are so adjusted as to prevent melting of the amorphized silicon layer by ion implantation during irradiation of the surface. Multiple-pulse laser annealing in the sub-melt regime of the amorphized silicon layer is adequate to activate the dopants and reduce the junction sheet resistance. Due to short annealing time and the absence of melting of the amorphous silicon layer, there is negligible dopant profile widening".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amended 4th paragraph on page 6 is new matter and reads as follows: "Laser parameters are so adjusted as to prevent melting of the amorphized silicon layer by ion implantation during irradiation of the surface. Multiple-pulse laser annealing in the sub-melt regime of the amorphized silicon layer is adequate to activate the dopants and reduce the junction sheet resistance. Due to short annealing time and the absence of melting of the amorphous silicon layer, there is negligible dopant profile widening".

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-7, 10-13, 16-18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong et al. (U.S. Patent No. 6,335,235 dated 1/1/2002), in view of Downey (U.S. Patent No. 6,878,415 filed 4/12/2005).

Chong shows the method substantially as claimed in Figs. 1-10 and 24 -26 and corresponding text as: forming a pre-amorphized implant layer (38) in between shallow trench isolation regions (14) and adjacent to the gate electrode structure (22) on a semiconductor substrate (10) (Fig. 5)(col. 5, lines 19-36); performing ion implantation (46) in said pre-amorphized implant layer to form source/drain extension regions (54) (Fig. 7) (col. 5, lines 55-67); and performing a sequential dual step annealing of said source/drain extension regions (Fig. 25) (col. 11, lines 24-47) (claim 1) (Fig. 24-26 refer to additional processing steps cared out after the initial steps of Figs. 1-10 are carried out). Chong teaches that the pre-amorphitization implantation is done with ions comprising Ge^+ or Si^+ (col. 5, lines 19-36) (claim 2). Chong teaches that the Ge+ or Si+ ion implant ion energy is approximately between 1 keV and 20 keV and the dose is approximately between 1E14 and 1E16 ions/cm^2 (col. 5, lines 38-44)(claim 3). Chong teaches that the SDE implant is done with B^+ ions (col. 5, lines 60-61) (claim 4). Chong teaches that the B+ ion implant energy is approximately between 0.2 keV and 0.7 keV and the dose is approximately between 5E14 and 1E16 ions/cm^2 (col. 5, lines 60-67) (claim 5). Chong teaches that the sequential dual step anneal comprises low temperature anneal followed by rapid thermal anneal (col. 10, line 61- col. 11, line 12) (col. 11, lines 24-47)(claim 6). Chong teaches that the low temperature annealing is done with laser irradiation (col. 10, line 61-col. 11, line 12) (claim 7). Chong teaches that

the rapid thermal anneal is done at approximately between 800°C and 1200°C for a duration of approximately between 0 sec and 60 sec (col. 11, lines 24-47) (claim 10). Chong shows the method as claimed in Figs. 1-10 and 24-26 and corresponding text as: forming a pre-amorphized Ge^+ or Si^+ implant layer in between shallow trench isolation regions and adjacent to gate electrode structure on a silicon substrate (Fig.5) (col. 5, lines 19-36); performing B^+ ion implantation in said pre-amorphized implant layer to form source/drain extension regions (col. 5, lines 55-67); and performing a sequential dual step annealing of said source/drain extension regions comprising low temperature laser anneal and rapid thermal anneal (RTA) (col. 10, line 61-col. 11, line 12) (col. 11, lines 24-47) (claim 11). Chong teaches that the Ge+ or Si+ ion implant ion energy is approximately between 1 keV and 20 keV and the dose is approximately between 1E14 and 1E16 ions/cm^2 (col. 5, lines 38-44)(claim 12). Chong teaches that the B+ ion implant energy is approximately between 0.2 keV and 0.7keV and the dose is approximately between 5E14 and 1E16 ions/cm^2 (col. 5, lines 55-67) (claim 13). Chong teaches that the rapid thermal anneal is done at approximately between 800°C and 1200°C for a duration of approximately between 0 sec and 60 sec (col. 11, lines 24-47) (claim 16). Chong shows the method as claimed in Figs. 1-10 and 24 -26 and corresponding text as: performing B+ ion implantation in a pre-amorphized implant layer to form source/drain extension regions on a silicon substrate (col. 5, lines 55-67); and performing a sequential dual step annealing of said source/drain extension regions comprising low temperature laser anneal and rapid thermal anneal (col. 10, line 61-col. 11, line 12) (col. 11, lines 24-47) (claim 17). Chong teaches that the B+ ion implant

energy is approximately between 0.2 keV and 0.7keV and the dose is approximately between 5E14 and 1E16 ions/cm^2 (col. 5, lines 55-67) (claim 18). Chong teaches that the rapid thermal anneal is done at approximately between 800°C and 1200°C for a duration of approximately between 0 sec and 60 sec (col. 11, lines 24-47) (claim 21).

Chong lacks anticipation only in not explicitly teaching that: 1) a sequential dual step sub-melt regime is used in annealing of said source/drain extension regions (claim 1); 2) he sequential dual step sub-melt regime anneal comprises low temperature anneal followed by rapid thermal anneal (claim 6); 3) the low temperature annealing is done with laser irradiation so as to not melt said pre-amorphized implant layer (claim 7); 4) a sequential dual step is used in annealing of said source/drain extension regions comprising low temperature sub-melt regime laser anneal and rapid thermal anneal (claim 11); and 5) a sequential dual step is used in annealing of said source/drain extension regions comprising low temperature sub-melt regime laser anneal and rapid thermal anneal (claim 17).

Downey teaches the activation of dopant material on a substrate using short-time thermal processes. The doped surface layer is irradiate with laser energy by a sub-melt laser, wherein the laser energy parameters are selected to produce the desired reaction between the surface layer and the dopant material without melting of the surface layer or the substrate (col. 6, lines 3-18). This procedure is used to avoid significant diffusion into the substrate (col. 2, lines 40-49).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to, modify Chong, by implementing a sub-melt regime anneal, as

taught by Downey, with the motivation that Downey teaches that a sub-melt laser anneal is used to avoid significant diffusion into the substrate.

8. Claims 8, 14, 19, 22-24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong et al. (U.S. Patent No. 6,335,235 dated 1/1/2002), in view of Downey (U.S. Patent No. 6,878,415 filed 4/12/2005) as applied to claims 1,11 and 17 above, and further in view of Yamazaki et al. (U.S. Patent No. 6,423,586, dated 7/23/2002).

Chong as modified by Downey shows the method substantially as claimed and as described in the preceding paragraphs.

Additionally, Chong shows that: 1) the Ge+ or Si+ ion implant ion energy is approximately between 1 keV and 20 keV and the dose is approximately between 1E14 and 1E16 ions/cm^2 (col. 5, lines 38-44)(claim 23). 2) Chong teaches that the B+ ion implant energy is approximately between 0.2 keV and 0.7keV and the dose is approximately between 5E14 and 1E16 ions/cm^2 (col. 5, lines 55-67) (claim 24); and 3) the rapid thermal anneal is done at approximately between 800°C and 1200°C for a duration of approximately between 0 sec and 60 sec (col. 11, lines 24-47) (claim 26).

Chong as modified by Downey lacks anticipation only in not explicitly teaching that: 1) the low temperature laser anneal is done using a multiple-pulsed 248 nm KrF excimer laser beam (claims 8, 15 and 19); 2) the multiple-pulsed laser beam has a pulse duration of approximately between 10 nsec and 40 nsec, and a repetition rate of 1-1000 pulses (claims 9, 16 and 20); 3) performing a sequential dual step annealing of said source/drain extension regions comprising low temperature multiple-pulsed laser

anneal and rapid thermal anneal (claim 22); and 4) the multiple-pulsed laser beam is a 248 nm KrF excimer laser with a pulse duration of approximately between 10 nsec and 40 nsec, and a repetition rate of 1-1000 pulses(claim 25).

Yamazaki teaches a method of annealing an amorphous semiconductor region in order to crystallize the area. Yamazaki uses a KrF excimer laser that has a 248 wavelength, which has a pulse duration of 10 nsec, an irradiation energy of 100 mJ, and a pulse repetition of 50 pulses, to effect the film annealing (col. 9, lines 29-36). The impurity areas, which were made amorphous by ion implantation, are then recrystallized (col. 9, lines 29-36). Then the semiconductor undergoes a thermal process to further crystallize the layer (col. 9, lines 37-49). The process helps to create high carrier mobility and provides a process with excellent reproducibility (col. 2, lines 21-29).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method shown in Chong as modified by Downey, by implementing a multiple-pulsed 248 nm KrF excimer laser beam, that has a pulse duration of approximately between 10 nsec and 40 nsec and a repetition rat of 1-1000 pulses as uses in Yamazaki, with the motivation that Yamazaki teaches that the process helps to create high carrier mobility and provides a process with excellent reproducibility.

9. Claims 9, 15, 20 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong et al. (U.S. Patent No. 6,335,253 dated 1/1/2002) in view of Downey (U.S. Patent No. 6,878,415 filed 4/12/2005) and Yamazaki et al. (U.S. Patent No. 6, 423,586, dated 7/23/2002) as applied to claims 8, 14, 19 and 22 above, and further in view of Talwar et al. (U.S. Patent No. 5,908,307 dated 6/1/1999).

Chong, as modified by Downey and Yamazaki shows the method as substantially claimed in the preceding paragraphs.

Chong, as modified by Downey and Yamazaki lacks anticipation by not explicitly teaching that: 1) the multiple-pulsed laser beam has a fluence of approximately between 0.1 J/cm^2 and 0.4 J/cm^2 (claims 9, 15, 20, 25).

Talwar describes the recrystallization of an amorphous silicon region that has been doped by a excimer laser anneal. The recrystallization of the amorphous layers are carried out with a pulsed 248 nm KrF laser (col. 5, lines 23-36). The fluence of the laser irradiation extends from 0.05 J/cm^2 to 1.0 J/cm^2 with the optimal irradiation level being 0.4 J/cm^2 (col. 6, lines 1-6). This process helps to eliminate high parasitic resistances and shorts between the junctions and the wells (col. 1, lines 44-64). Also the number of point defects is decreased after the laser anneal process (col. 7 lines 1-8).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method shown in Chong, as modified by Downey and Yamazaki to implement the fluence as being approximately between 0.1 J/cm2 and 0.4 J/cm2 as taught by Talwar with the motivation that Talwar teaches that at an irradiation level of 0.4 J/cm2 the process eliminates high parasitic resistances and shorts between the junctions and the wells. Additionally, Talwar shows a decrease in point defects after the laser anneal.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
August 6, 2005